UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,347	04/27/2001	Jun Zeng	SE1645PD (50042)	2463

7590 04/19/2004

CHRISTOPHER F. REGAN, ESQUIRE
ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST, P.A.
P.O. Box 3791
Orlando, FL 32802-3791

EXAMINER	
SOWARD, IDA M	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,347	ZENG, JUN	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicants amendment filed March 3, 2004.

Claim Objections

Claims 23, 32 and 36 are objected to because of the following informalities: "**non-interruptibly**" should have been **non-interruptively** in lines 12, 13 and 13, respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 23, 26, 32 and 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not understood how the dielectric layer extends outwardly from the semiconductor layer, the source regions and the source/body contact regions, and the outwardly extending dielectric layer having sidewalls aligned with sidewalls of the trench.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

As best understood, claims 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Willaims et al. (US 2002/0019099 A1).

In regard to claim 23, Willaims et al. teach a MOSFET comprising: a semiconductor layer having a trench therein; a gate conducting layer in a lower portion of the trench; a dielectric layer in an upper portion of the trench; source regions 159 adjacent the dielectric layer; source/body contact regions 160 laterally spaced apart from the gate conducting layer and non-interruptibly contacting the source regions; the dielectric layer extending outwardly from the semiconductor layer, the source regions and the source/body contact region, and the outwardly extending dielectric layer having

sidewalls aligned with sidewalls of the trench (Figure 15D, pages 8-9, paragraphs [0118]-[0122]).

In regard to claim 24, Williams et al. teach a source electrode on the source regions and on the dielectric layer (Figure 15D, pages 8-9, paragraphs [0118]-[0122]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willaims et al. (US 2002/0019099 A1) as applied to claims 23-24 above, and further in view of Pitzer et al. (WO 97/07548).
Williams et al. teach all mentioned in the rejection above. However, Williams et al. fail to teach at least one conductive via between the source electrode and the source/body contact regions. In regard to claim 25 and as best understood of claim 32, Pitzer et al. teach at least one conductive via between the source electrode 52 and the source/body contact regions 34 (Figure 2, page 7, lines 3-36). Since Williams et al. and Pitzer et al. are from the same field of endeavor (trenched MOSFET devices), the purpose disclosed by Pitzer et al. would have been pertinent in the art of Williams et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the trenched MOSFET of Williams et al. with the trenched MOSFET having conductive vias as taught by Pitzer et al. to provide a MOSFET with improved threshold control (page 1, lines 5-9).

As best understood, claims 26-27 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willaims et al. (US 2002/0019099 A1) as applied to claims 23-24 above, and further in view of Marchant et al. (US 2003/0060013 A1).

Williams et al. teach all mentioned in the rejection above. In regard to claim 27, Williams et al. further teach a source electrode 158 on the source regions 159, on the dielectric layer, and on the source/body contact regions 160, a gate dielectric layer lining the trench. However, Williams et al. fail to teach a portion of the source regions including an opening exposing the source/body contact regions, wherein the source/body contact regions are exposed by an opening in the source region. Marchant et al. teach a portion of the source regions 202 & 402 including an opening exposing the source/body contact regions 200 & 400, wherein the source/body contact regions are exposed by an opening in the source region; a source electrode 116 on the source region 402, on the dielectric layer 114 and on the source/body contact regions 200; a portion of the source regions 402 including a recess over the source/body contact regions 404 (Figures 2B and 4, pages 2-3, paragraphs [0014] and [0019]). Since Williams et al. and Marchant et al. are from the same field of endeavor (trenched MOSFET devices), the purpose disclosed by Marchant et al. would have been pertinent in the art of Williams et al. Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to modify the trenched MOSFET of Williams et al. with the trenched MOSFET having openings as taught by Marchant et al. to improve transistor ruggedness without compromising transistor comprising transistor cell pitch (abstract).

As best understood, claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US 2002/0019099 A1) as applied to claims 23-24 above, and further in view of Kocon et al. (US 6,351,009 B1).

Williams et al. teach all mentioned in the rejections above. However, Williams et al. fail to teach an outwardly extending dielectric layer extending from a source region equal to or less than about 1 micron. Kocon et al. teach an outwardly extending dielectric layer 111 extending from a source region 106 from 0.5 to 0.8 microns, which is within the range of equal to or less than about 1 micron (Figure 1, col. 2, lines 2-4). Since Williams et al. and Kocon et al. are from the same field of endeavor (MOSFET devices), the purpose disclosed by Kocon et al. would have been pertinent in the art of Williams et al. Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made to modify the MOSFET of Williams et al. with the MOSFET having an outwardly extending dielectric layer extending from a source region as taught by Kocon et al. to minimize source-to-gate capacitance (col. 1, lines 63-67).

As best understood, claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US 2002/0019099 A1) as applied to claim 23-24 above, and further in view of Mo et al. (US 6,710,406 B2).

Williams et al. teach all mentioned in the rejections above. However, Williams et al. fail to teach a gate recessed in the trench within a range of 0.2 to 0.8 microns from the opening thereof. Mo et al. teach a gate 28 recessed in the trench 14 within a range of 0 to 0.4 microns, which is in the range of 0.2 to 0.8 microns (Figures 1A-1B, col. 4, lines 64-67). Since Williams et al. and Mo et al. are from the same field of endeavor (MOSFET devices), the purpose disclosed by Mo et al. would have been pertinent in the art of Williams et al. Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made to modify the MOSFET of Williams et al. with the FET having the gate and source/body contact region recess depth as taught by Mo et al. to provide a device with excellent reliability (col. 2, lines 11-19).

As best understood, claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US 2002/0019099 A1) as applied to claims 23-24 above, and further in view of Han et al. (5,891,776).

Williams et al. teach all mentioned in the rejection above. However, Williams et al. fail to teach the source/body contact regions recessed within the semiconductor layer adjacent the source regions. Han et al. teach a source/body contact region 17 recessed within a semiconductor layer 3 adjacent the source regions 19 (Figure 3A, col. 7, lines 9-67). Since Williams et al. and Han et al. are from the same field of endeavor

(MOSFET devices), the purpose disclosed by Han et al. would have been pertinent in the art of Williams et al. Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made to modify the MOSFET of Williams et al. with the MOSFET having recessed areas as taught by Han et al. to provide a MOSFET with a small unit cell size (col. 4, lines 17-19).

As best understood, claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US 2002/0019099 A1) and Han et al. (5,891,776) as applied to claim 23-24 and 30 above, and further in view of Mo et al. (US 6,710,406 B2).

Williams et al. and Han et al. teach all mentioned in the rejections above. However, Williams et al. and Han et al. fail to teach an upper surface of the recess of the source/body contact region 34 equal to or less than 1 micron from a surface of the semiconductor layer. Mo et al. teach an upper surface of the recess of the source/body contact region 34 equal to or less than 1 micron shown by 16 in comparison to the recessed trench (Figures 1A, col. 4, lines 64-67). Since Williams et al., Han et al. and Mo et al. are from the same field of endeavor (MOSFET devices), the purpose disclosed by Mo et al. would have been pertinent in the art of Williams et al. and Han et al. Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made to modify the MOSFET of Williams et al. and the MOSFET having recessed areas as taught by Han et al. with the FET having the gate and source/body contact region recess depth as taught by Mo et al. to provide a device with excellent reliability (col. 2, lines 11-19).

As best understood, claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Willaims et al. (US 2002/0019099 A1) and Pitzer et al. (WO 97/07548) as applied to claims 23-25 and 32 above, and further in view of Marchant et al. (US 2003/0060013 A1).

Williams et al. and Pitzer et al. teach all mentioned in the rejections above. However, Williams et al. and Pitzer et al. fail to teach a recess over the source/body contact regions wherein the source/body contact regions are recessed within the semiconductor layer adjacent the source regions. Han et al. teach a portion of the source regions 19 including a recess over the source/body contact regions 17 wherein the source/body contact regions are recessed within the semiconductor layer 3 adjacent the source regions 19 (Figure 3A, col. 7, lines 9-67). Since Williams et al., Pitzer et al. and Han et al. are from the same field of endeavor (MOSFET devices), the purpose disclosed by Han et al. would have been pertinent in the art of Williams et al. and Pitzer et al. Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made to modify the MOSFET of Williams et al. and MOSFET having conductive vias of Pitzer et al. with the MOSFET having recessed areas as taught by Han et al. to provide a MOSFET with a small unit cell size (col. 4, lines 17-19).

As best understood, claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US 2002/0019099 A1) and Pitzer et al. (WO 97/07548) as applied to claims 23-25 and 32 above, and further in view of Kocon et al. (US 6,351,009 B1).

Williams et al. and Pitzer et al. teach all mentioned in the rejections above. However, Williams et al. and Pitzer et al. fail to teach an outwardly extending dielectric layer extending from a source region equal to or less than about 1 micron. Kocon et al. teach an outwardly extending dielectric layer 111 extending from a source region 106 from 0.5 to 0.8 microns, which is within the range of equal to or less than about 1 micron (Figure 1, col. 2, lines 2-4). Since Williams et al., Pitzer et al. and Kocon et al. are from the same field of endeavor (MOSFET devices), the purpose disclosed by Kocon et al. would have been pertinent in the art of Williams et al. and Pitzer et al. Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made to modify the MOSFET of Williams et al. and the MOSFET having conductive vias of Pitzer et al. with the MOSFET having an outwardly extending dielectric layer extending from a source region as taught by Kocon et al. to minimize source-to-gate capacitance (col. 1, lines 63-67).

As best understood, claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US 2002/0019099 A1) and Pitzer et al. (WO 97/07548) as applied to claim 23-25 and 32 above, and further in view of Mo et al. (US 6,710,406 B2).

Williams et al. and Pitzer et al. teach all mentioned in the rejections above. However, Williams et al. and Pitzer et al. fail to teach a gate recessed in the trench within a range of 0.2 to 0.8 microns from the opening thereof. Mo et al. teach a gate 28 recessed in the trench 14 within a range of 0 to 0.4 microns, which is in the range of 0.2

to 0.8 microns (Figures 1A-1B, col. 4, lines 64-67). Since Williams et al., Pitzer et al. and Mo et al. are from the same field of endeavor (MOSFET devices), the purpose disclosed by Mo et al. would have been pertinent in the art of Williams et al. and Pitzer et al. Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made to modify the MOSFET of Williams et al. and the MOSFET having conductive vias of Pitzer et al. with the FET having the gate and source/body contact region recess depth as taught by Mo et al. to provide a device with excellent reliability (col. 2, lines 11-19).

As best understood, claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Willaims et al. (US 2002/0019099 A1) and Marchant et al. (US 2003/0060013 A1) as applied to claims 23-24, 26-27 and 36-37 above, and further in view of Kocon et al. (US 6,351,009 B1).

Williams et al. and Marchant et al. teach all mentioned in the rejections above. However, Williams et al. and Marchant et al. fail to teach a dielectric layer extending from a region equal to or less than about 1 micron. Kocon et al. teach an outwardly extending dielectric layer 111 extending from a source region 106 from 0.5 to 0.8 microns, which is within the range of equal to or less than about 1 micron (Figure 1, col. 2, lines 2-4). Since Williams et al., Marchant et al. and Kocon et al. are from the same field of endeavor (MOSFET devices), the purpose disclosed by Kocon et al. would have been pertinent in the art of Williams et al. and Pitzer et al. Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made

to modify the MOSFET of Williams et al. and the MOSFET having openings as taught by Marchant et al. with the MOSFET having an outwardly extending dielectric layer extending from a source region as taught by Kocon et al. to improve the switching speed (col. 1, lines 63-67).

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US 2002/0019099 A1) and Marchant et al. (US 2003/0060013 A1) as applied to claims 23-24, 26-27 and 36-37 above, and further in view of Mo et al. (US 6,710,406 B2).

Williams et al. and Marchant et al. teach all mentioned in the rejections above. However, Williams et al. and Marchant et al. fail to teach a gate recessed in the trench within a range of 0.2 to 0.8 microns from the opening thereof. Mo et al. teach a gate 28 recessed in the trench 14 within a range of 0 to 0.4 microns, which is in the range of 0.2 to 0.8 microns (Figures 1A-1B, col. 4, lines 64-67). Since Williams et al., Marchant et al. and Mo et al. are from the same field of endeavor (MOSFET devices), the purpose disclosed by Mo et al. would have been pertinent in the art of Williams et al. and Pitzer et al. Therefore, it would have been obvious to one having ordinary skill in the ad at the time the invention was made to modify the MOSFET of Williams et al. and the MOSFET having openings as taught by Marchant et al. with the FET having the gate and source/body contact region recess depth as taught by Mo et al. to provide a device with excellent reliability (col. 2, lines 11-19).

Response to Arguments

Applicant's arguments with respect to claims 23-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to trenched MOSFETs:

Brush et al. (US 6,246,090 B1) Mo (US 2002/0038886 A1)

Sapp (US 6,351,018 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
March 29, 2004

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800